## AMENDMENTS TO THE DRAWINGS

The August 21, 2008 Final Office Action objected to the drawings under 37 C.F.R. § 1.83(a) as not showing every feature of the invention specified in the claims. The Final Office Action also objected to Figure 4 for containing an unlabeled box between gate electrode 9 and drain contact 16.

In response to these objections, Applicant has amended Figures 2 and 4, which amendments are contained in two (2) Replacement Sheets submitted herewith. Applicant respectfully submits that no new matter has been added by the amended drawings.

## REMARKS

The August 21, 2008 Final Office Action was based on pending Claims 1–11. By this Response, Applicant is amending Claims 1, 3, 8 and 11 without prejudice or disclaimer, and Claims 2, 4–7, 9 and 10 remain as previously presented. Thus, after entry of the foregoing amendments, Claims 1–11 are pending and presented for further consideration. In view of the foregoing amendments and the remarks set forth below, Applicant respectfully submits that Claims 1–11 are in condition for allowance.

## AMENDMENTS TO THE DRAWINGS

The Final Office Action has provided a number of objections to the drawings. As discussed above, Applicant has amended Figures 2 and 4, which amendments are contained in two (2) Replacement Sheets submitted herewith. Applicant respectfully submits that no new matter has been added by the amended drawings. The details of the amendments follow below.

Regarding Claim 1, the Final Office Action states that Claim 1 requires that "the further metal strip is locally **electrically connected** to the metal source contact and the connection between the two is made of a capacitor" (emphasis added). The Final Office Action further states that Figure 5 shows the further metal strip connected to a capacitor but not the further metal strip's connection to the metal source contact.

Applicant respectfully emphasizes that the Claim 1 recites "electrically connected." Applicant points out that the source contact (15) is connected to source zone (4), which is short-circuited with the p-type region via a deep, strongly-doped p-type zone (11). The strongly-doped p-type zone (11) extends from the surface down to the strongly-doped substrate (2), which connects the source zone (4) to the source electrode (12) at the lower side of the substrate via the substrate (2) (see, e.g., Paragraph 0025 of the published application—U.S. Patent Publication No. 2006-0220154), thereby providing the source potential to the source contact (15).

Likewise, with reference to Figure 3, "[t]he upper electrode (31) is connected, via metal plugs (34) and an additional metal layer (37) incorporated therein, to a polycrystalline silicon region (99)," and the second plate of capacitor (30) "is formed by

the portion of the semiconductor body (1) that is present under a thin oxide layer (36), in this case a portion of the epitaxial layer (3) and the substrate (2), which electrode is connected to the source connection (12)," and thus is at source potential (Paragraph 0028).

In Figure 5, the capacitor electrodes are formed by (31) and (32). Lower electrode (32) is electrically connected through silicide region (35) and strongly-doped (p-type) semiconductor region (36) to the p-doped silicon region (2) (like zone (11)) (Paragraph 0023).

Regarding Claim 2, Applicant has amended Figure 2 to show active region (6) (also shown in Figure 4) with the capacitor (30) (and electrode (31)) positioned within the active region beside the transistor. Active region (6) is formed by the interdigitated structure repeatedly containing (4,15), (9,18), (20) and (16,5) for each digit of the structure (see, e.g., Paragraph 0002).

Regarding Claim 3, Applicant has amended Claim 3 to conform to the description in Paragraph 0028, which states that the further metal strip (20) is formed in the lower layer of the two metal layers, according to the figures as pointed out by the Examiner.

Regarding Claim 8, Applicant has amended Claim 8 to state "that the metal strips serving as the contacts of the source zone, the drain zone and the gate electrode are embodied as parallel metal strips positioned beside each other," as pointed out by the Examiner to conform to Figure 2.

Regarding Figure 4, Applicant has amended Figure 4 to clarify that the unmarked box represents the further metal strip (20), which extends upward to connect to the capacitor (see, e.g., in Figure 3).

## CLAIM REJECTIONS UNDER 35 U.S.C. § 112, SECOND PARAGRAPH

The Final Office Action rejected Claim 1 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention, In particular, the Office Action indicated that Claim 1 is unclear because "the disclosure and the drawings teach the

metal source contact, drain contact and gate electrode contact being the metal strips, not there being additional metal strips that connect the source zone, drain zone and gate electrode to their respective contacts."

Applicant thanks the Examiner for pointing out the error in the wording of the claim and has amended the wording to conform to the description in the application (see, e.g., Paragraph 0002). In particular, Applicant has replaced the word "via" with "in the form of" in accordance with the description.

As indicated above, Claim 8 has also been amended to clarify wording based on similar logic. In both cases, no new matter has been added.

**CLAIM REJECTIONS UNDER 35 U.S.C. § 103(a)**

The Final Office Action rejected Claims 1–11 as being unpatentable over U.S. Patent No. 6,069,386 to Jos ("Jos") in view of U.S. Patent No. 6,294,798 to Zambrano ("Zambrano"). Applicant respectfully traverses this rejection, the characterization of the pending claims, and each an every implicit and/or explicit official notice. Moreover, in view of the foregoing amendments and for at least the reasons set forth below, Applicant respectfully disagrees and requests reconsideration of Claims 1–11.

**Independent Claim 1**

Claim 1 recites, among other things, "that the electrical connection **between the further metal strip and the metal source contact** comprises a capacitor" (emphasis added).

Jos appears to teach insertion of a further metal strip (20) in a semiconductor device (see, e.g., Figure 1 and col. 3, lines 32–63). However, as acknowledged by the Examiner, Jos does not teach or suggest attaching a capacitor between the further metal strip and a source contact.

Rather, in Jos the further metal strip (20) serves as a capacitive screening between a gate strip (18) (also referred to as track (18) – see col. 3, line 34) and a drain strip (16) (also referred to as track (16)). The further metal strip (20) is connected to source connection (12) via strip (15) by means of connection (21). Jos does not disclose or suggest that the electrical connection (i.e., (21) and (15)) between the

further metal strip (20) and the source contact (12) comprise a capacitor. Additionally, neither the strip (15) nor the connection (21) is suggested to serve as a capacitor in any way. Therefore, Jos does not teach or suggest the above limitation.

Zambrano appears to teach forming a circuit structure on a semiconductor substrate, which comprises electronic devices formed with both CMOS technology elements and capacitor elements (see, e.g., col. 1, line 58 through col. 2, line 12). Zambrano aspires to form an integrated circuit with contact areas with a low aspect ratio and better integrated so that the overall circuit structure will be more compact relative to prior art (see, e.g., col. 1, lines 58–65). Specifically, Zambrano describes two embodiments in which its capacitor is connected between the source and the drain of a MOS transistor (see, e.g., col. 2, line 26 through col. 4, line 49 (with particularity in col. 2, lines 62–64 and col. 4, lines 42–46)).

It may be possible that a skilled artisan may conclude from Zambrano to create integrated circuits with the capacitor included in a compact form, wherein the capacitor is connected between the source and the drain, or possibly even between other contacts of a transistor (e.g., the gate contact) as may be practiced in non-integrated circuits.

However, Zambrano does not teach or suggest electrically connecting capacitors for no apparent reason between a further metal strip that is insulated from the semiconductor body and the source contact of the semiconductor, as recited by Claim 1.

Applicant describes and claims adding a capacitor, whether integrated or not, (see, e.g., Paragraphs 0006 and 0007) to the further metal strip, and has found such to provide unexpected results as described in Applicant's specification, specifically as illustrated in Figures 6, 7 and 8 and as further described in Paragraphs 0029 and 0031–0033. One skilled in the art would not have had any reason to connect a capacitor to the further metal strip taught by Jos.

Since neither Jos, nor Zambrano, nor a combination thereof, teaches or suggests each and every element of amended independent Claim 1, the Final Office Action has not shown a prima facie case of obviousness as required by M.P.E.P.

§ 2143.03. Therefore, Applicant respectfully requests allowance of independent Claim 1.

**Claims 2–11**

Claims 2–11 depend from independent Claim 1 and are believed to be patentably distinguished over the cited references for the reasons set forth above with respect to Claim 1 and for the additional features recited therein.

Moreover, Claim 11 has been amended for grammatical reasons so that it would be in correct form for allowance.

**Summary**

The amendments to the claims presented herein have been introduced to place the claims in correct form for allowance or appeal, based on the remarks presented in the August 21, 2008 Final Office Action. The amendments do not add new matter or affect the merits of the claim, and do not place an additional burden on the Examiner. Therefore Applicant respectfully requests their entry after final.

**NO DISCLAIMERS OR DISAVOWALS**

Although the present communication may include alterations to the application or claims, or characterizations of claim scope or referenced art, Applicant is not conceding in this application that previously pending claims are not patentable over the cited references. Rather, any alterations or characterizations are being made to facilitate expeditious prosecution of this application. Applicant reserves the right to pursue at a later date any previously pending or other broader or narrower claims that capture any subject matter supported by the present disclosure, including subject matter found to be specifically disclaimed herein or by any prior prosecution. Accordingly, reviewers of this or any parent, child or related prosecution history shall not reasonably infer that Applicant has made any disclaimers or disavowals of any subject matter supported by the present application.

## CONCLUSION

In view of the foregoing, the present application is believed to be in condition for allowance, and such allowance is respectfully requested. If further issues remain, the Examiner is cordially invited to contact the undersigned such that the issues may be promptly resolved.

Moreover, by the foregoing amendments and remarks no admission is made that any of the above-cited references are properly combinable. Rather, Applicant submits that even if the references are combined, the references still do not teach or suggest the claimed invention.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

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